Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.An electrostatic discharge (ESD) protection device having reduced trigger voltage, comprising:

a substrate of first conductivity type;

a first MOS transistor of second conductivity type disposed on said substrate, said first MOS transistor comprising a first gate, a first gate dielectric disposed under said first gate, a first heavily doped region of said second conductivity type implanted into said substrate at one side of said first gate, and a second heavily doped region of said second conductivity type implanted into said substrate at the other side of said first gate;

a second MOS transistor of said second conductivity type laterally disposed on said substrate in proximity to said first MOS transistor, said second MOS transistor comprising a second gate, a second gate dielectric disposed under said second gate, a third heavily doped region of said second conductivity type implanted into said substrate at one side of said second gate, and a fourth heavily doped region of said second conductivity type implanted into said substrate at the other side of said second gate; and

at least one floating gate MOS transistor comprising a floating gate dielectric formed on said substrate and a floating gate overlying said floating gate dielectric, said floating gate MOS transistor being located between said first MOS transistor and said second MOS transistor, wherein said floating gate MOS transistor is serially connected to said first MOS transistor via said second heavily doped region and is connected to said second MOS transistor via said third heavily doped region.

[c2] 2.The ESD protection device according to claim 1 wherein said first heavily doped region is contiguous with a first lightly doped drain (LDD) of said second conductivity type that is under said first gate, said second heavily doped region is contiguous with a second LDD of said second conductivity type that is under said first gate, and a first channel of said second conductivity type is defined between said first LDD and said second LDD under said first gate.

[c3] 3.The ESD protection device according to claim 1 wherein said third heavily doped region is contiguous with a third LDD of said second conductivity type that is under said second gate, said fourth heavily doped region is contiguous with a fourth LDD of said second conductivity type that is under said second gate, and a second channel of said second conductivity type is defined be-

tween said third LDD and said fourth LDD under said second gate.

[c4] 4.The ESD protection device according to claim 1 wherein said second heavily doped region is contiguous with a fifth LDD of said second conductivity type that is under said floating gate, said third heavily doped region is contiguous with a sixth LDD of said second conductivity type that is under said floating gate, and a third channel of said second conductivity type is defined between said fifth LDD and said sixth LDD under said floating gate.

[c5] 5.The ESD protection device according to claim 1 wherein said first gate dielectric and said second gate dielectric have a first thickness, and said floating gate dielectric has a second thickness, wherein said first thickness is not equal to said second thickness.

[c6] 6.The ESD protection device according to claim 5 wherein said first thickness is larger than said first thickness.

[c7] 7.The ESD protection device further comprising halo implant regions of said first conductivity type disposed in said substrate under said fifth LDD and said sixth LDD respectively.

[c8] 8.The ESD protection device according to claim 1 wherein said first conductivity type is P type, and said second conductivity type is N type, and wherein, in operation, said substrate, said first gate, said second gate, said first heavily doped region, and said fourth heavily doped region are all grounded, said floating gate remains floating, and said second heavily doped region, which is electrically connected with said third heavily doped region, is connected to input/output power terminal.

[c9] 9.The ESD protection device according to claim 1 wherein said first conductivity type is N type, and said second conductivity type is P type, and wherein, in operation, said substrate, said first gate, said second gate, said first heavily doped region, and said fourth heavily doped region are connected to V_{DD}, said floating gate remains floating, and said second heavily doped region, which is electrically connected with said third heavily doped region, is connected to input/output power terminal.

[c10] 10.An electrostatic discharge (ESD) protection device having reduced trigger voltage, comprising:

a P type substrate;

a first NMOS transistor disposed on said substrate, said

first NMOS transistor comprising a first gate, a first gate dielectric disposed under said first gate, a first N^+ doped region implanted into said substrate at one side of said first gate, and a second N^+ doped region implanted into said substrate at the other side of said first gate;

a second NMOS transistor laterally disposed on said substrate in proximity to said first NMOS transistor, said second NMOS transistor comprising a second gate, a second gate dielectric disposed under said second gate, a third N^+ doped region implanted into said substrate at one side of said second gate, and a fourth N^+ doped region implanted into said substrate at the other side of said second gate, wherein said first gate dielectric and said second gate dielectric has substantially the same thickness: first thickness; and

at least one floating gate MOS transistor comprising a floating gate dielectric formed on said substrate and a floating gate overlying said floating gate dielectric, said floating gate MOS transistor being located between said first NMOS transistor and said second NMOS transistor, wherein said floating gate MOS transistor is serially connected to said first NMOS transistor via said second N^+ doped region and is serially connected to said second NMOS transistor via said third N^+ doped region, and wherein said floating gate dielectric has a second thickness, and said second thickness is smaller then said first

thickness.

[c11] 11.The ESD protection device according to claim 10 wherein said first N^+ doped region is contiguous with a first NLDD that is under said first gate, said second N^+ doped region is contiguous with a second NLDD that is under said first gate, and a first N channel is defined between said first NLDD and said second NLDD under said first gate.

[c12] 12.The ESD protection device according to claim 10 wherein said third N^+ doped region is contiguous with a third NLDD that is under said second gate, said fourth N^+ doped region is contiguous with a fourth NLDD that is under said second gate, and a second N channel is defined between said third NLDD and said fourth NLDD under said second gate.

[c13] 13.The ESD protection device according to claim 10 wherein said second N^+ doped region is contiguous with a fifth NLDD that is under said floating gate, said third N^+ doped region is contiguous with a sixth NLDD that is under said floating gate, and a third N channel is defined between said fifth NLDD and said sixth NLDD under said floating gate.

14.The ESD protection device according to claim 10 further comprising P^+ halo implant regions disposed in said

substrate under said fifth NLDD and said sixth NLDD respectively.

[c14] 15.The ESD protection device according to claim 10 wherein in operation, said substrate, said first gate, said second gate, said first N^+ doped region, and said fourth N^+ doped region are all grounded, said floating gate remains floating, and said second N^+ doped region, which is electrically connected with said third N^+ doped region, is connected to input/output power terminal.